IN THE CLAIMS

1. (Original) A method of fault resilient booting in a multiprocessor system, comprising:

designating one processor as a bootstrap processor;

testing the bootstrap processor to verify that it will run BIOS code;

setting a latch for disabling said bootstrap processor if the testing indicates a failure;

testing during a power on self-test the operation of said bootstrap processor;

testing during a built-in self-test the operation of said bootstrap processor;

assigning the bootstrap process to another processor if said bootstrap processor fails a test;

said testing steps being implemented in an appliance server management system.

2. (Previously Presented) The method according to claim 1, wherein testing the bootstrap processor comprises using a timer which indicates a failure if the bootstrap processor is not reset within a predetermined time.

3. (Original) The method according to claim 2, wherein a failure in the second or third testing step also causes said latch to be set.

4. (Original) The method according to claim 1, wherein the testing steps are controlled by a control unit.

5. (Original) The method according to claim 4, wherein the control unit includes the system I/O chip.

6. (Original) An apparatus for fault resilient booting, comprising:

a first processor designated as a bootstrap processor;

a latch for turning off said bootstrap processor;

a control unit for providing control signals for setting said latch, for resetting said latch and for controlling additional processors.

7. (Original) The apparatus according to claim 6, further comprising a timer for determining if said bootstrap processor is operating properly.

8. (Original) The apparatus according to claim 7, wherein said timer begins a time period wherein power is turned on and ends said time period after a predetermined time.

9. (Original) The apparatus according to claim 8, wherein the bootstrap processor is considered to fail if said timer is not reset before reaching said predetermined time.

10. (Original) The apparatus according to claim 6, wherein said control unit includes a system I/O chip.

11. (Original) The apparatus according to claim 6, wherein the apparatus is part of an appliance server management system.

12. (Previously Presented) A multiprocessor system for fault resilient booting, comprising:

a plurality of processors with one processor being designated a bootstrap processor;

a control unit for generating a series of control signals;

a timer;

a latch for turning said bootstrap processor off;

said timer providing a signal indicating that a predetermined time has expired, which is applied to said latch to set said latch;

said control unit providing a first signal to said latch for setting said latch, a second signal applied to said latch for resetting said latch, a third signal for controlling other processors and a fourth signal for resetting the timer.

13. (Original) The system according to claim 12, wherein said first signal from said control unit is generated when said bootstrap processor fails a power-on self-test or a built-in self-test.

14. (Original) The system according to claim 12, wherein said timer tests whether said bootstrap processor can run BIOS code.

15. (Original) The system according to claim 12, wherein the system is part of an appliance server management system.

16. (Previously Presented) A system according to claim 12, wherein said control unit causes another processor to become the bootstrap processor when said bootstrap processor is disabled by said latch.